

A High Speed, Wide Dynamic Range Digital Data Acquisition System

Robert Auer¹, Bruce Weber², Eric Statler²
¹Advanced Technology Center, ²Biomedical Research,
 Beckman Coulter, Inc., Miami, Florida

ABSTRACT

We have previously reported on two generations of data acquisition systems for flow cytometric use which incorporated wide dynamic range active integration of the signals from the detectors and analog to digital conversion with fifteen bits of conversion resolution and twenty bits of effective dynamic range. These advances have permitted accurate computer normalization of complex dye emission spectra overlaps for multiple detectors and computer synthesis of accurate four decade logarithmic data with resolution of 256 channels per decade. We are now reporting on a third generation, higher speed data acquisition system which retains the above mentioned features of the original systems while substantially increasing the rate at which data can be acquired. The number of parameters that potentially can be acquired has also been increased from sixteen to forty eight; including pulse area, height, and width at a constant fraction of height for up to sixteen independent sensors. In addition, the number of independent laser intersection points has increased from three to up to five. The wide dynamic range uncompensated data is transferred to an external workstation via a 480 mbaud USB 2.0 link and stored in FCS 3.0 format file for subsequent off line processing.

INTRODUCTION

Historically, most sensor signals in flow cytometry have been digitized at a low to medium resolution (eight to ten bits) after the signals have been processed in the analog domain. This analog processing included passive pulse integration, peak capture, inter-channel subtraction to compensate for the spectral overlap of the fluorophores, and logarithmic amplification. Accurate compensation for the spectral overlap of more than two fluorescence detection channels requires the use of additive as well as subtractive coefficients, this results in very complex analog circuitry. All of these analog signal processing methods introduce inaccuracies in the recorded data due to inherent limitations in the analog circuitry. A method of reducing these inaccuracies is to convert the analog signals to digital values as early in the process as is practical and then to process the signals in the digital domain.

Direct digitization of detector waveforms has been reported since the early 1970's (1).

These systems were limited by the then available technology to slow particle velocities and low count rates. In 1993 (2,3) we introduced an analog/digital hybrid data acquisition system for flow cytometric use; which incorporated wide dynamic range, active integration and peak capture of the signals from the detectors in the analog domain. This analog waveform processing was followed by analog to digital conversion with fifteen bits of conversion resolution and twenty bits of effective dynamic range. This technique permitted digital compensation of complex dye emission spectra overlaps for multiple fluorescence detectors and computer synthesis of accurate logarithmic data with a range of four decades and at a resolution of 256 channels per decade. That system acquired seven parameters plus elapsed time at a maximum data rate of about three thousand events per second. Since then numerous systems have been reported that directly digitize the detector waveforms but they have not been able to equal the dynamic range and resolution of the analog/digital hybrid system due to the limitations of available analog to digital converters.

In 2002 we are reported on a second generation analog/digital hybrid data acquisition system which retained the wide dynamic range and high resolution of the earlier system while increasing the rate at which data can be acquired to over thirty thousand events per second. In addition, the number of parameters that could be acquired was increased from seven to sixteen plus elapsed time. The uncompensated wide dynamic range data was stored in a FCS format file for subsequent processing.

We are now reporting on a third generation, higher speed data acquisition system which retains the above mentioned features of the original systems while again increasing the rate at which data can be acquired. The number of parameters that can be acquired has also been increased from sixteen to forty eight; including pulse area, height, and width at a constant fraction of height for up to sixteen independent sensors. In addition, the number of independent laser intersection points has increased from three to up to five. The wide dynamic range uncompensated data is transferred to an external workstation via a 480 mbaud USB 2.0 link and stored in FCS 3.0 format file for subsequent off line processing.

THE ANALOG/DIGITAL HYBRID SYSTEM CONCEPT

The fundamental operation of the hybrid analog/digital data acquisition system is shown in figure one. The signal from the detector is amplified as required. It can then be routed to the data acquisition circuit card for use as a trigger to initiate a pulse capture sequence. The amplified signal enters a five microsecond delay line. This delay allows the trigger circuit to activate a pulse capture sequence prior to the pulse exiting the delay line, thus permitting the capture of the whole pulse. If a pulse capture sequence is initiated, the delayed pulse is captured by three analog processing circuits: a peak, sense, and hold circuit measures the peak amplitude of the pulse; an active integrator circuit, as shown in figure one, measures the area of the pulse; and a width at constant fraction of height circuit measures the width of the pulse at one half of its peak height.

The data acquisition circuit card controls the pulse capture sequence. A pulse capture sequence begins with the "OPEN" signal. This signal removes the short from the "capture" capacitor, allowing it to charge. The capture sequence ends with the "CLOSE" signal. This signal disconnects the pulse signal source from the capture circuit, thus protecting the captured signal from subsequent pulses. The "CLOSE" signal also causes the output of the capture circuit to be held in a first sample and hold circuit after a short delay to allow for settling. This first sample and hold circuit prevents any errors due to a droop in the voltage on the capture capacitor due to leakage currents. The information to be recorded about the pulse has now been converted from a time varying to a constant voltage.

The output of the first sample and hold circuit passes through two precision amplifiers, one has unity gain and the other has a gain of thirty two (2⁵). The output of the gain of thirty two amplifier is monitored by a comparator circuit, which compares the amplified constant voltage from the amplifier with a slowly changing triangular waveform which varies between two fixed positive values near to but below the maximum linear output voltage of the gain of thirty two amplifier.

Analog/Digital Hybrid Data Acquisition System

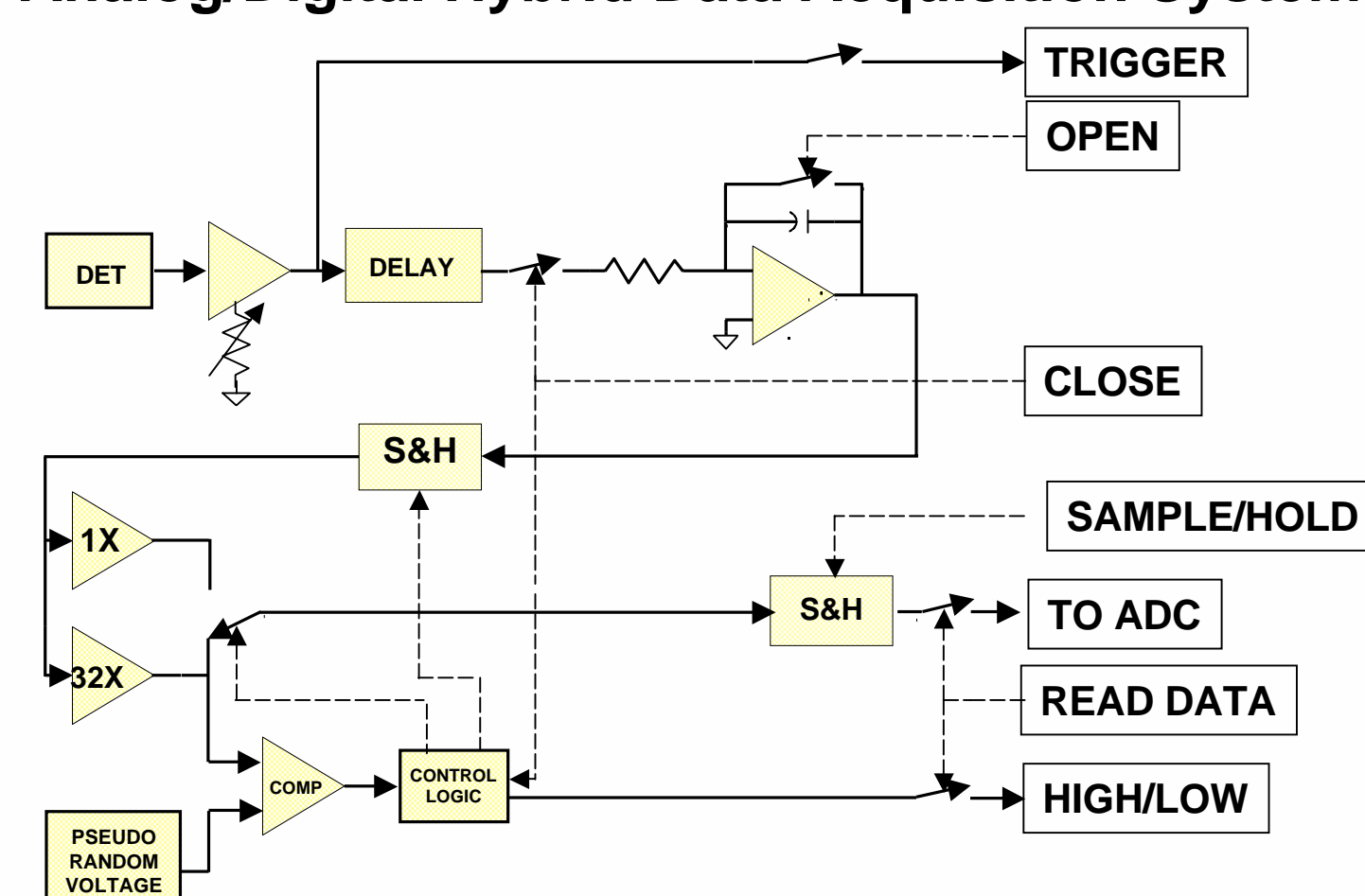


Figure One

If the output of the gain of thirty two amplifier is below the ramp voltage, then the output of the gain of thirty two amplifier is selected for digitization. If the output of the unity gain amplifier is above the ramp voltage, then the output of the unity gain amplifier is selected for digitization. Since the pulse events occur randomly with respect to the frequency of the triangular waveform, the exact decision point varies randomly from event to event. This averages out any small gain or offset errors between the two amplifiers.

The three resulting analog outputs are then digitized with a high resolution, sixteen bit analog to digital converter. The least significant bit is dropped to yield fifteen bits of converted resolution. Five bits are then appended to the least significant or the most significant ends of the fifteen converted data bits depending on which amplifier was used. If the gain of thirty two amplifier was used then the five bits are on the most significant end. If the unity gain amplifier was used then the data is shift up five bits. In either case a twenty bit final result is generated.

The New System

The design goal for the new system was to increase the maximum data acquisition rate to one hundred thousand events per second while increasing the number of parameters measured and the number of laser intersection points serviced. In order to accomplish this, the previous design was analyzed for throughput bottlenecks and design changes were made to improve the performance. The original sixteen bit analog to digital converter had a ten microsecond conversion time and was replaced with a device that has a one microsecond conversion time. This allows the digitization of three parameters in less time than it previously took for one. The galvanic isolators through which the parameter data is transferred to the USB interface were changed from optical couplers with a 350 ns signal delay to magnetic couplers with a 10 ns signal delay. All of the delay shift registers were changed from discrete parts to being synthesized in Complex Programmable Logic Devices (CPLDs) in order to increase their maximum clock speeds and increase their flexibility. All CPLD clock speeds were increased from 40 mhz to 80 mhz so that decisions could be made faster. All critical CPLDs were doubled in size to accommodate the logic to support the additional lasers.

Data Acquisition System

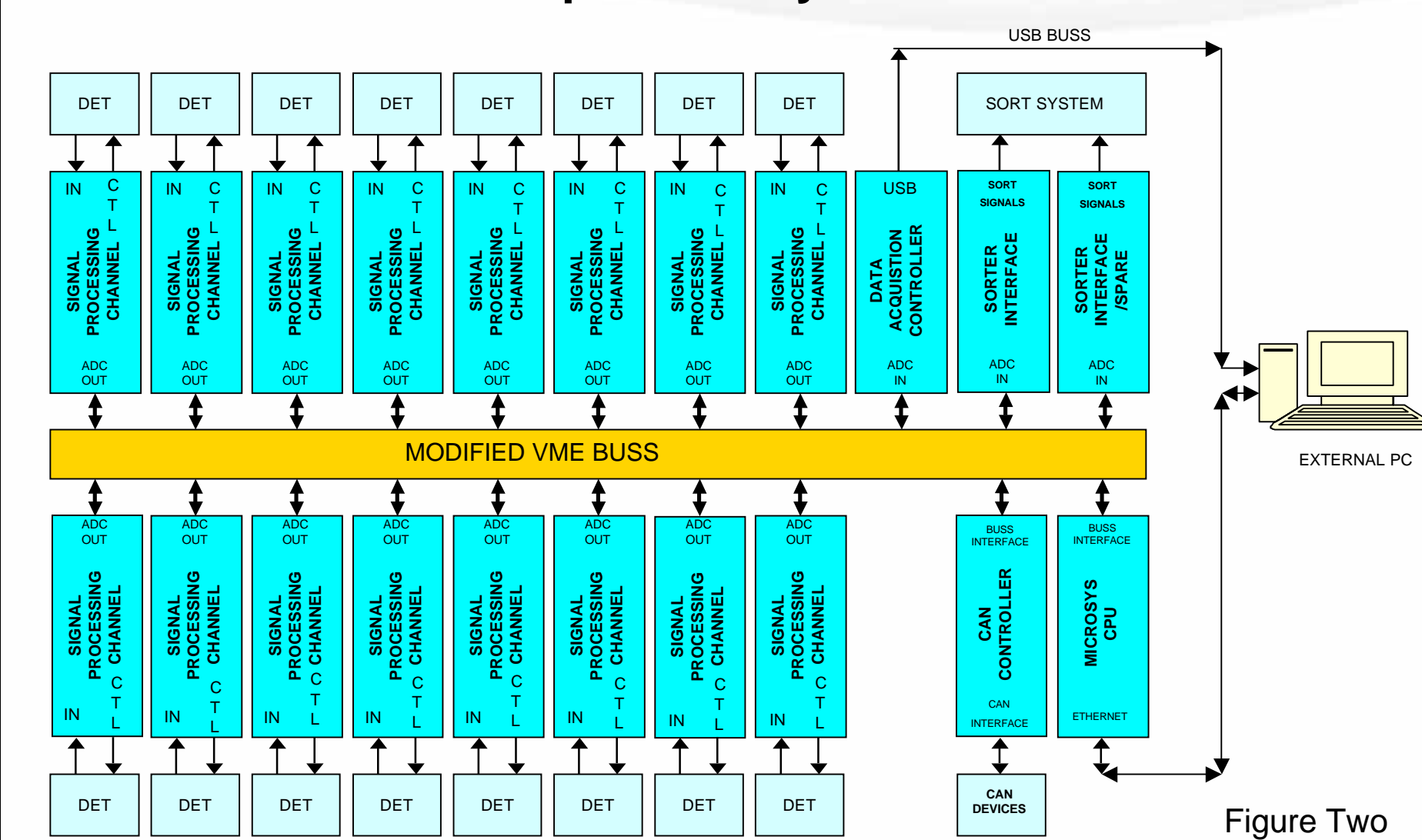


Figure Two

Figure two shows the over all block diagram of the system. It is composed of sixteen identical Signal Processors, each of which is connect a detector such as a photomultiplier or photodiode. The signal processors are controlled by a single Data Acquisition circuit card. Also located in the buss are the sorting interface circuit cards, a CAN controller for instrument control, and a microprocessor circuit card. The data acquisition circuit card and the microprocessor circuit card are both connected to an external PC via independent communication paths, one for data and the other for command and control. Figure three shows the interconnections between a typical Signal Processor and the Data Acquisition cards.

Interconnect Block Diagram

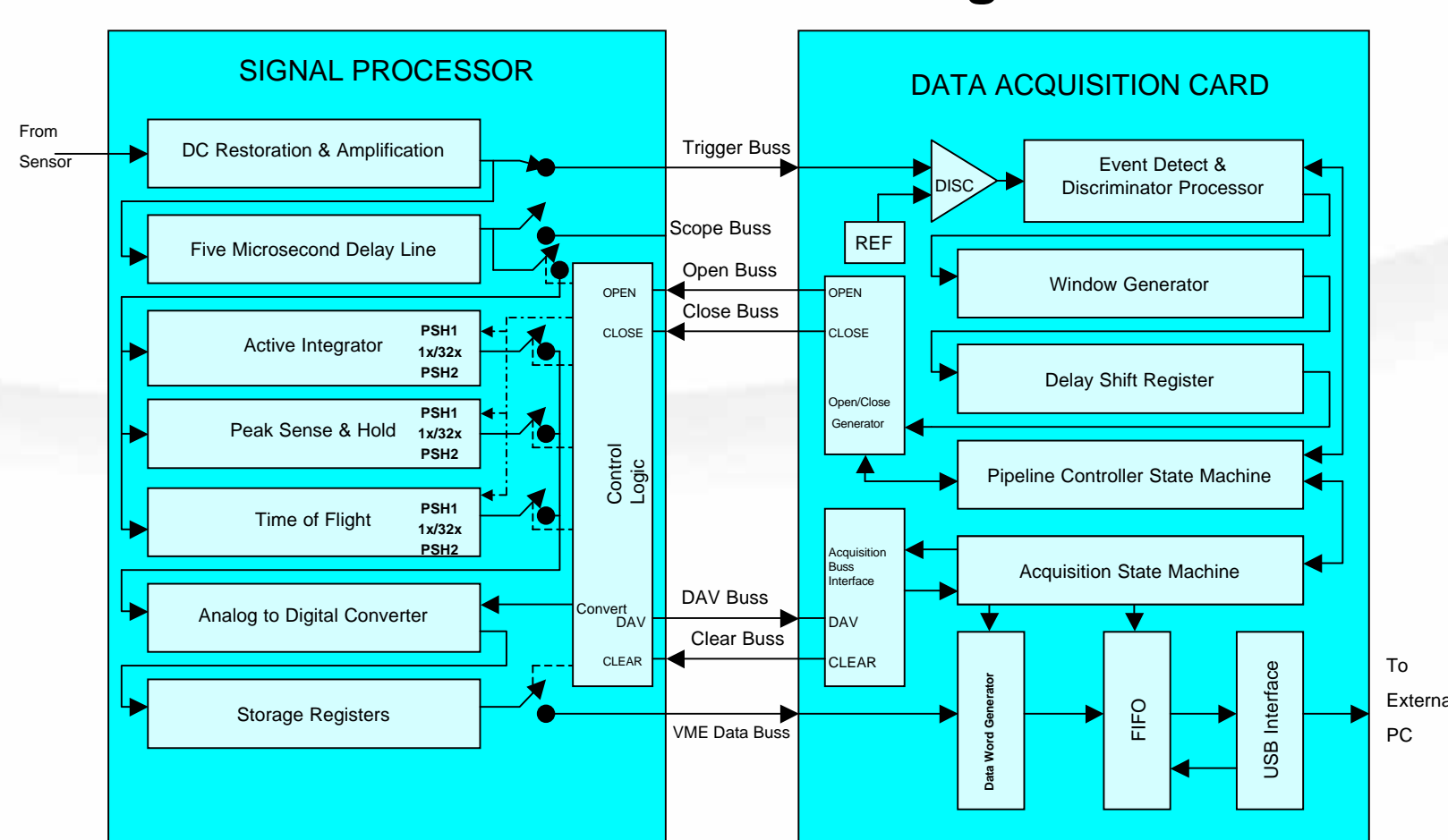


Figure Three

Signal Processing Block Diagram

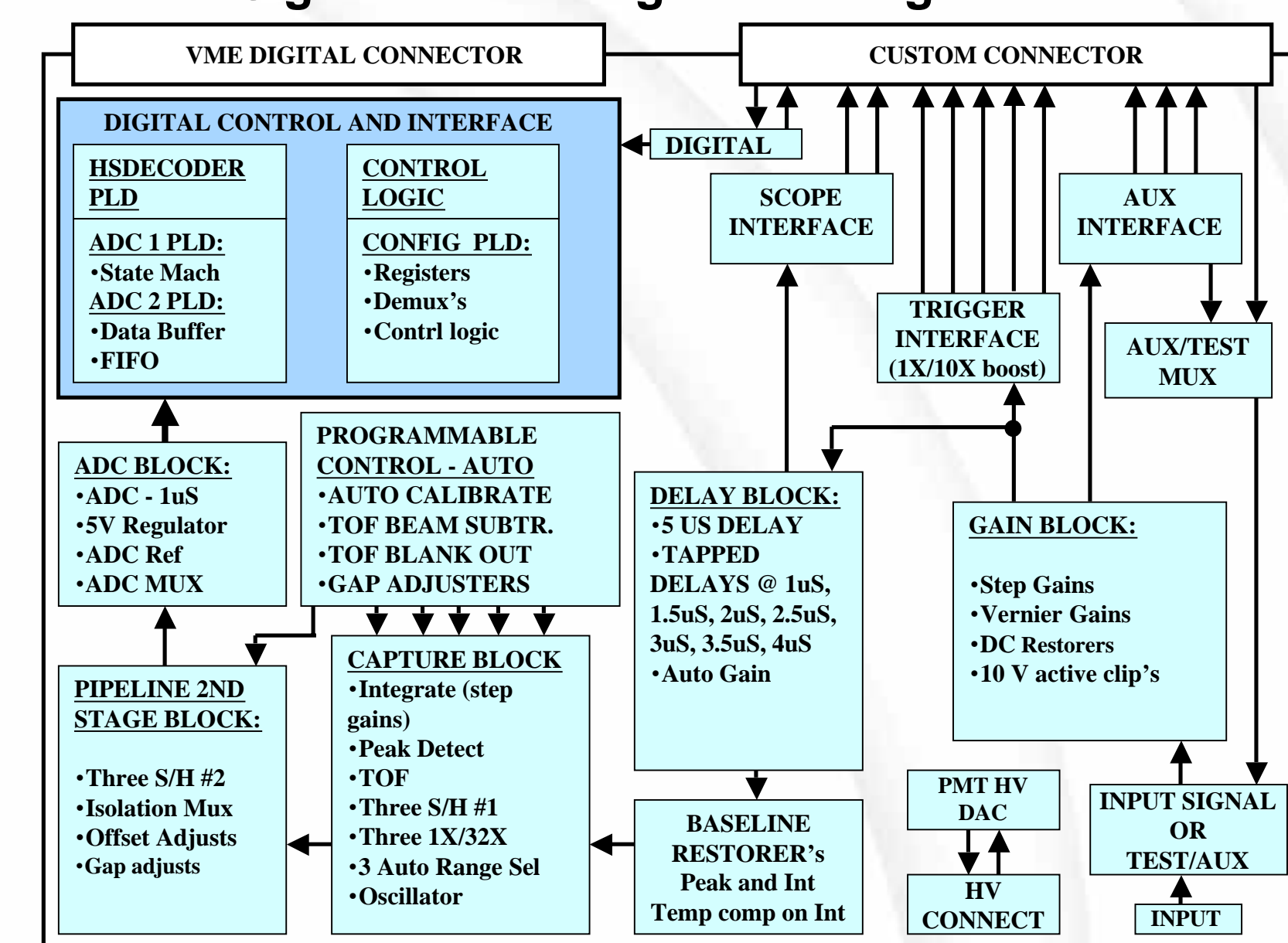


Figure Four

Data Acquisition Block Diagram

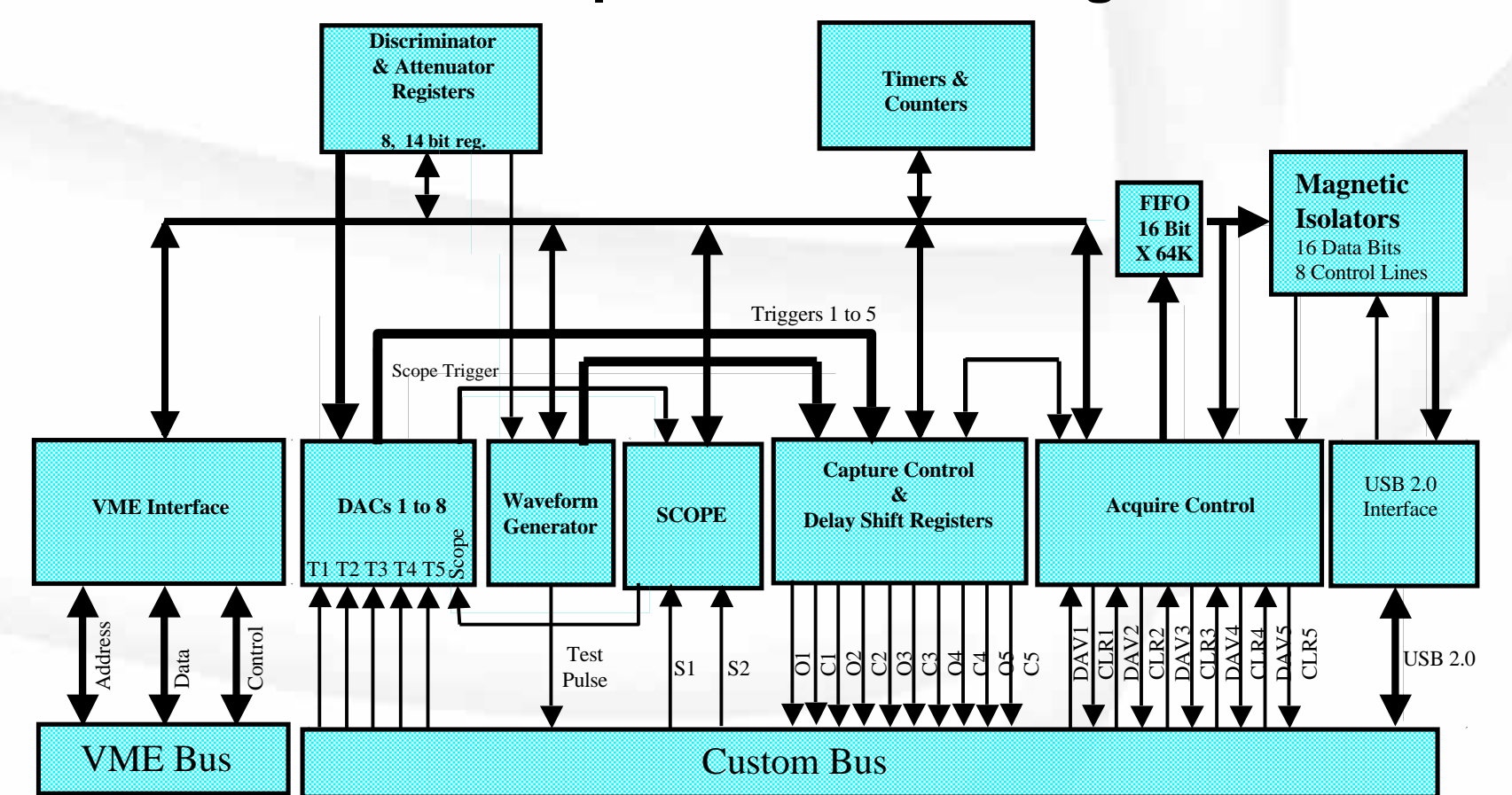


Figure Five

Figures four and five show the internal block diagrams of the Signal Processor and the Data Acquisition circuit cards.

Multiple Laser Timing Diagram

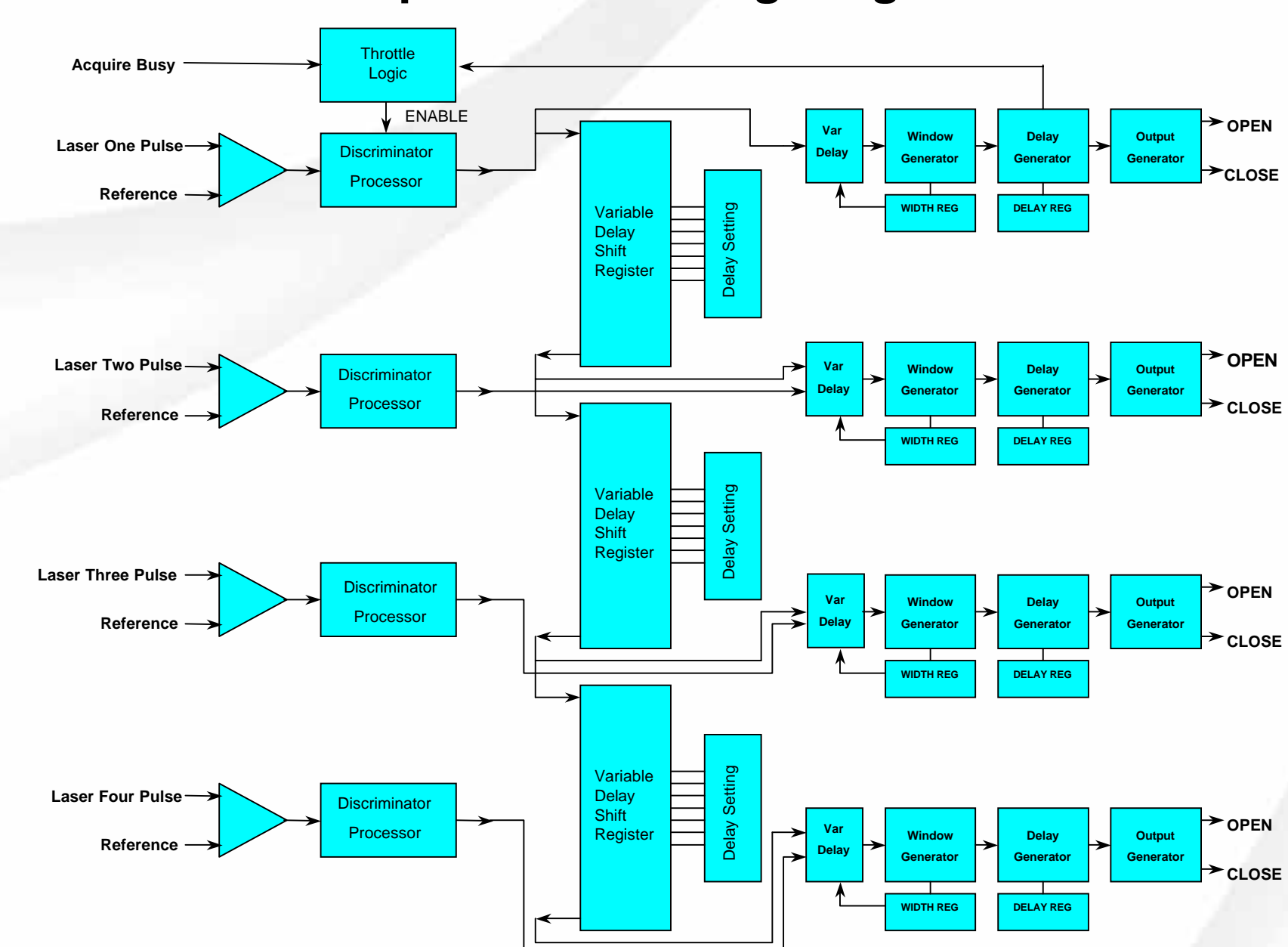


Figure Six

Figure six shows a four laser configuration of the Capture Pipeline. Qualified discriminator satisfied signals from the first laser propagate down a segmented delay line, whose segment lengths are equal to the time between each laser beam. At each beam location the propagated discriminator satisfied signal can be programmed to either trigger an acquisition sequence directly or to gate the signal from a local discriminator. In the second mode a timer forces a cycle if a local discriminator signal is not detected within a programmed window of time.

The segmented delay line can accommodate multiple qualified laser one discriminator satisfied signals at the same time permitting the pipelining of multiple events through the capture system. The throttle logic monitors the number of events that have entered the segmented delay line, the spacing between them, and the status of the acquisition system in order to qualify the laser one discriminator signals and permit them to enter the segmented delay line. The throttle logic limits the number of events processed to those that are far enough apart to be independently captured and also prevents overrun in the signal processors. Each signal processor can pipeline three events; one in its output registers, one in the A to D conversion process, and one in the capture process. The converted data from all of the Signal Processor is read and written into a deep FIFO and from there goes to the USB interface. The actual capture rate of the system is dependent on the sheath velocity of the flow system. As the sheath velocity increases, both the time in the beams and the time between the beams decreases. This shrinks the width of the capture windows and the length of the segmented delay line permitting the system to cycle faster.

REFERENCES

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3. US Patent 5,367,474